AN ADAPTIVE NEURAL SPIKE THRESHOLD SENSOR USING NOISE RMS VOLTAGE IN .18μm CMOS

by

Andrew Duffield

APPROVED BY SUPERVISORY COMMITTEE:

Dr. Jin Liu, Chair

Dr. Hoi Lee

Dr. Jeong-Bong Lee

# AN ADAPTIVE NEURAL SPIKE THRESHOLD SENSOR USING NOISE RMS VOLTAGE IN .18μm CMOS

by

ANDREW BRUCE DUFFIELD, B.S.E.E.

THESIS

Presented to the Faculty of

The University of Texas at Dallas

in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT DALLAS

December, 2008

*To my parents, my brother, and my wonderful wife to be*

ACKNOWLEDGEMENTS

I would like to express my gratitude to my research advisor, Dr. Jin Liu. She has been a source of encouragement and guidance these past years. She has been approachable and supportive, tolerant of my shortcomings, has praised my abilities when my faith in them faltered, and vouched on my behalf when my own words were insufficient. She has guided my research while encouraging individual progress and study. My mentorship with her has given me valuable knowledge and confidence, which I believe are the core of a real education. For this opportunity, I am very thankful.

I would like to thank Dr. Jeong-Bong Lee for his contributions to the wireless transmitter used with the chip described herein, and for taking the time to read and respond to my thesis, and for sitting on my advisory committee.

I would also like to thank Dr. Hoi Lee for sitting on my advisory committee during a very busy period, for reading and discussing my thesis with me, and for acting as a liaison when communication between committee members became difficult.

Thanks also go to my peers in the Analog and Mixed Signal IC Design groups at UTD. They have provided valuable help, and feedback. They each have a bright future waiting for them. Particular thanks go to the members who worked on the implantable wireless neural sensor: Jun Yuan, Diana Yan, and Junjie Yao.

And finally, I would like to thank my family: my parents, who raised me and pushed me to be better, whom I must repay by realizing my potential, my brother, who listened when I was frustrated, and for whom I must set an example, and my fiancée Gift, who has shown me endless love and support, for whom I do everything I do, to make myself worthy of such a remarkable young woman.

July, 2008

AN ADAPTIVE NEURAL SPIKE THRESHOLD SENSOR USING NOISE RMS VOLTAGE IN .18μm CMOS

Publication No. _____

Andrew Bruce Duffield, M.S.E.E.
The University of Texas at Dallas, 2008

Supervising Professor: Dr. Jin Liu

Human prosthetics in the near future will require communication with the nervous system. It is therefore necessary to create implantable devices that can read electrical information sent by the brain. The Analog Design Team at the University of Texas at Dallas has developed a prototype chip that can be powered wirelessly and communicate with an external interface through the skin, eliminating the need for battery maintenance and skin breaks for communication. It is designed to be connected to the peripheral nerves that previously controlled the lost limb, thus minimizing rehabilitation. This thesis describes an adaptive neural spike threshold sensor used on the chip to determine an appropriate threshold level for nerve spikes. The RMS level of the noise in the nerve signal is used to set the threshold. The sensor dissipates 2 μW, has an area of 1.77mm$^2$ and incorporates a novel charge pump based approach to setting the threshold.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

# CHAPTER 1

# INTRODUCTION

The size of integrated circuits has continued to shrink ever since their invention in 1958. Advances in the field have resulted in denser memory arrays, cheaper production, and functionality that previously seemed like science fiction. Computer processors boast 3 GHz + operation with as many as 4 cores in the consumer sector, with options scaling higher still in the business sector. And with higher performance still than computer processors, dedicated signal processors achieve performance orders of magnitude higher in their respective disciplines.

With such advanced integrated circuits, it's a wonder that they haven't been applied more widely in the medical field. In fact, it is only recently that large silicon companies have started to consider medical applications to be one of their major revenue sources. Integrated circuits have become fairly mature, and are now ready for medical applications that demand great sensitivity.

The medical sector is traditionally slow to adopt new technologies, but demand for proven medical services remains stable and grows predictably. From the point of view of an investor accustomed to volatility and rapid growth in tech markets, or to a silicon company searching for the next big market, the slow-to-change medical field may appear to be an underperforming investment. However, as bursting technology bubbles have illustrated in the past, it is often wiser to invest in areas with solid, consistent growth. Sales of silicon to producers of medical equipment show just such a trend. Because there is very little public excitement surrounding the sector, and healthcare is affected by economic fluctuations less than

other sectors, growth is very consistent and predictable. However, over a 10 year span, growth is far from slow.

For people with amputated limbs, even tasks that seem trivial to most people can be difficult, frustrating, or even impossible when appropriate tools are unavailable. As a society possessing the technology to print an integrated circuit on each and every bag of potato chips, fabricate computers the size of fingernails, and (most importantly) develop application specific IC's that cheaply perform almost any function imaginable, a moral imperative exists for us to advance technology that could help those who have endured amputations. As Mahatma Ghandi put it, "A nation's greatness is measured by how it treats its weakest members." And certainly, a nation that helps the handicapped lead normal lives with minimal frustration shows its greatness.

The Analog Integrated Circuit Design Team at UTD seeks to develop an implantable integrated circuit that can be used to establish wireless communication between the human peripheral nervous system and an external electronic device, with the long term intention of allowing the nervous system to control a prosthetic device. Eventually, such devices could restore autonomy and mobility to amputees, not only in the first world, but also in war affected and poor countries where people often have little recourse when maimed.

### 1.1 Wireless Implantable System Overview

The overall project is a collaborative effort between several members of the Analog Integrated Circuit Design group at the University of Texas at Dallas, of which the author is a member, Zyvex, and other parties. The chip was developed with funding and information from Zyvex, while they perfected a technique for stimulating perhipheral nerve growth into tubes and onto contacts. That project in turn was sponsored by DARPA. This paper addresses a subcircuit

of the chip, the adaptive threshold circuit, which can function as part of the overall system or independently.

The goal of the project is to create a small, animal-implantable silicon sensor chip with 128 channels, each of which is capable of detecting a nerve firing and wirelessly transmitting that data over a short distance using an inductive coupling through the skin. That data would then be received by an auxiliary device on the outside of the skin. The intended application is a prosthetic limb that can receive data from a sensor implanted underneath the skin near the amputation site. The sensor chip is intended to be powered wirelessly, much like an RFID chip, so that connecting a power source through the skin or implanting a battery in the patient becomes unnecessary.

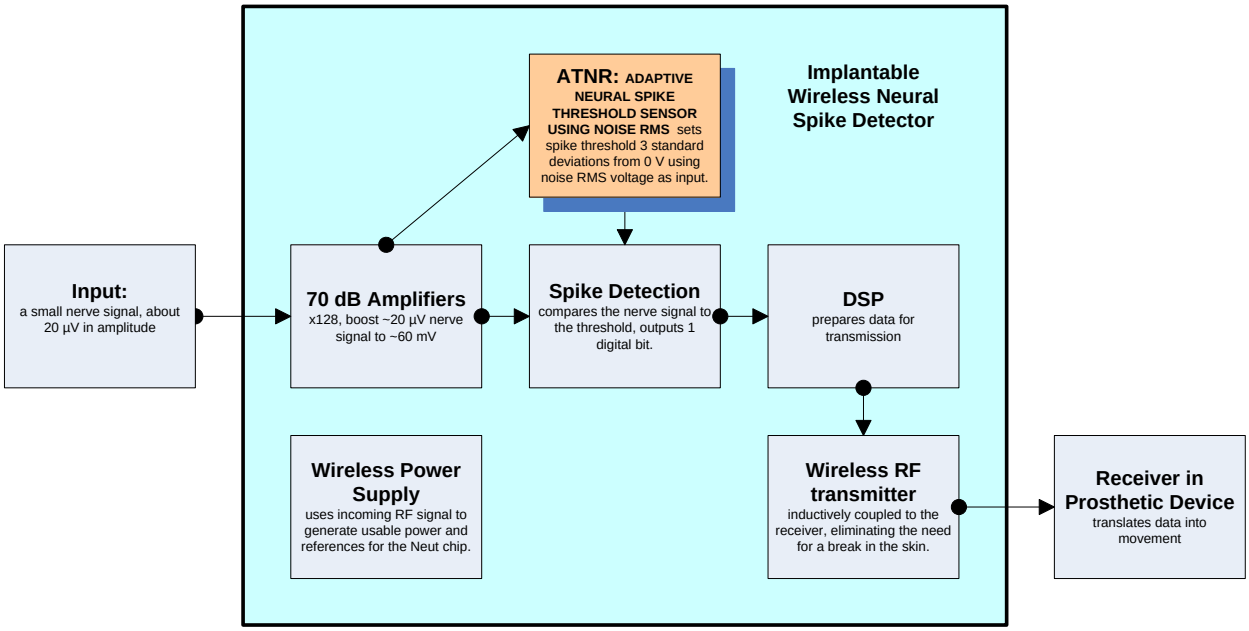



**Figure 1.1. Wireless Implantable System at Block Level**

Tasks that must be performed by the sensor chip include: the rectification of wireless energy and generation of a stable DC power source, the amplification of roughly 30 µV nerve signals to a level that can be interpreted by sensor circuitry, determination of a threshold level to

separate nerve spikes from noise, comparison of the signal with the threshold level, digital processing to filter out likely false positives, serialization and transmission of the data back out across the same wireless link that captures the power from the auxiliary system. The auxiliary system that sends power to the sensor chip, receives data from the sensor chip, and interfaces with the prosthetic itself is outside the scope of UTD's analog design team's undertaking.

### 1.2 Goal of Adaptive Threshold Circuit

The raw firehose of incoming nerve data must be processed into some reasonable form before it can be transmitted over the wireless link. Because up to 128 channels are being monitored, this places significant demands on the bandwidth of the link. Analog wireless transmission would result in distortion of the signal and/or exceed the available bandwidth, and using an ADC to create a sufficiently detailed digital representation of the nerve waveform would also violate the bandwidth constraint. Therefore, some form of data reduction is required.

In this implementation, the input signal coming from the nerve is compared to a reference level in order to determine whether the signal is a spike. This "spike or no spike" bit can then be serialized with the other 128 channels of data and transmitted at much lower bandwidth cost. Determining such a reference level is challenging, because nerve data can vary greatly in shape and magnitude. The amount and shape of noise present also varies greatly. Therefore, an appropriate reference level cannot be supplied that will work for all circumstances. It must be determined dynamically, on chip.

The goal of the adaptive threshold portion of the chip is to constitute a reasonable spike threshold level based on the amount of noise present in the input signal. If the threshold is too low, spike detection will be too sensitive, and many false positives will appear. Set the threshold too high and no spikes will be detected. Since the input signal only has a signal to noise ratio of

about 3 to 1, a constant threshold cannot be set without first observing the input noise. Furthermore, there is inherent variation among biological systems that makes an adaptive threshold system indispensable. Environmental noise, plus the noise introduced by the amplifier attempting to read such a small input signal must be eliminated.

The goal of this thesis is to find a solution to this problem, by examining a very noisy analog input signal, and determining an appropriate threshold level for spikes based on the amount of noise present in the input.

## CHAPTER 2

## BACKGROUND REVIEW

A nerve signal contains a large amount of environmental noise, plus additional noise from the input amplifier. In order to determine whether a signal spike is present at a given moment in time, it is helpful to know the normal range in which the signal resides; that is, the highest and lowest values that are likely to be present during the normal quiet portion of the signal, that is, the portion with no signal spikes, but where noise is still present. The noise power is more helpful to a circuit designer when expressed as root mean square (RMS) noise voltage. A simple definition of noise RMS voltage over an arbitrary measurement period $T_M$ is given below [4, 620]:

$$V_{nRMS} = \sqrt{V_n^2} = \sqrt{\lim_{T_M \to \infty} \int_{T_1}^{T_1 + T_M} v_n^2(t)\,dt} \tag{1}$$

Or, for a general signal with defined bounds in time $T_1$ and $T_2$,

$$V_{RMS} = \sqrt{\frac{1}{T_2 - T_1} \int [V(t)]^2 dt} \tag{2}$$

To detect the RMS level of a voltage signal V(t), a designer must first consider carefully the type of signal being analyzed. If the signal is periodic (or otherwise deterministic), he can make a simple calculation based on the known parameters of the signal. For example, with a little calculus, the RMS voltage level of a sine wave can be found to be [1, 411]:

$$V_{RMS} = \sqrt{\frac{1}{T_{period}} \int_0^T \left[V_{peak} \cos(\omega t)\right]^2 dt} = \sqrt{\frac{V_{peak}^2}{2T}\left[t - \sin\left(\frac{2\pi t}{T}\right)\cos\left(\frac{2\pi t}{T}\right)\right]_0^T} = \frac{V_{peak}}{\sqrt{2}} \tag{3}$$

However, if the signal V(t) is a sampled stochastic process, the RMS voltage cannot be computed in this fashion. Define the sampled signal V(x) to be a set of voltage samples from the signal V(t). The standard deviation σ of a set of points is defined as the root mean square of the distance of each point from the arithmetic mean of the set, as shown below [6, 170]:

$$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}[x_i - \mu]^2} \tag{4}$$

μ is defined as the mean value of the set. Notice the similarity of equation (4) to (2). If a zero mean is assumed for the set, σ appears to be the discrete equivalent of $V_{RMS}$. In other words, the RMS voltage level of a signal is the expected, or standard, deviation from the mean level, which will be 0 in our discussion of electrical signals.

If it is further assumed that the input signal is stationary, each sample in V(x) is a Gaussian random variable, and 68.27% of the samples will (likely) lie within 1σ, or RMS level, of the mean. Considering that 15.87% of samples that are less than μ-1σ, 84.14% of samples lie below the level μ+1σ. Therefore, if a level can be found below which 84.14% of the samples lie and above which 15.87% of samples lie, then this must be the 1σ or $V_{RMS}$ level. This level will be referred to as the 1σ level. A hypothetical 1σ is illustrated in figure 2.1.

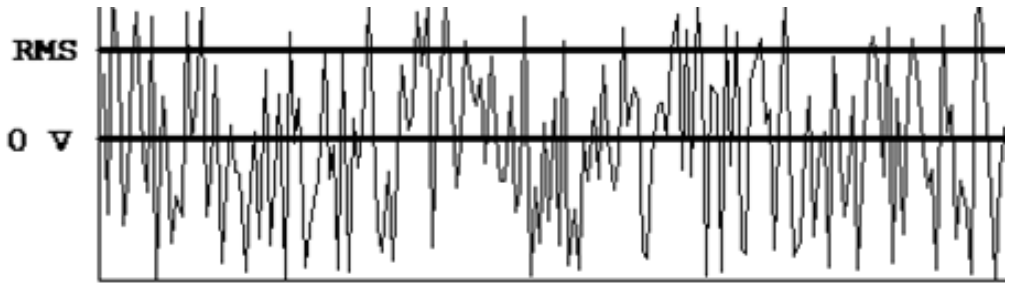



**Figure 2.1. RMS voltage is roughly equivalent to 1 standard deviation**

## 2.2 A Feedback Based "RMS" Detection Algorithm

In [2], Harrison presents a method for setting the threshold of a nerve spike based on the RMS level of the noise present in the channel. Harrison presents a feedback algorithm to determine an approximate 1σ level, as shown in figure 2.2.

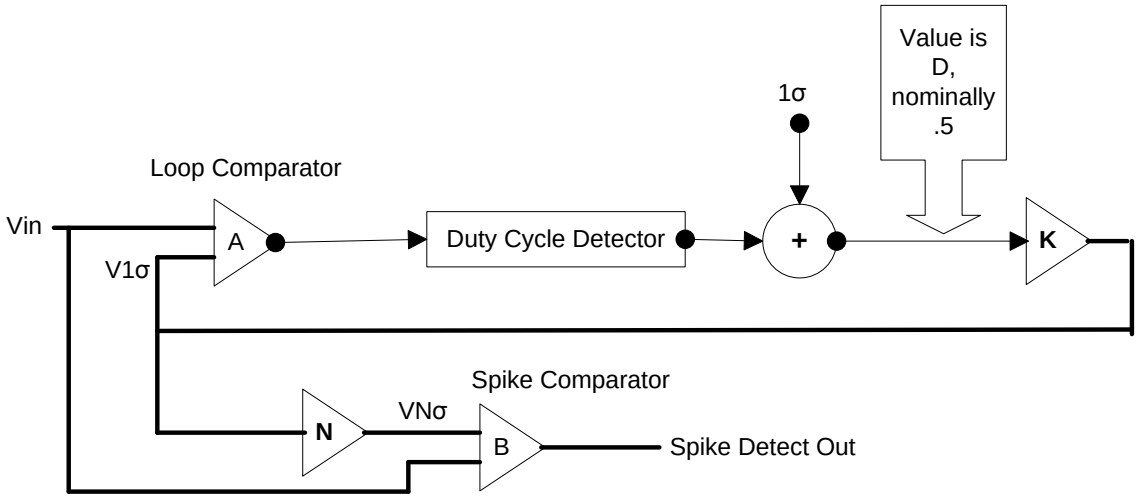



**Figure 2.2. Harrison's feedback based RMS detection algorithm**

A loose linear interpretation of the algorithm is given here. Gain A is assumed for the loop comparator and duty cycle estimator, and D describes the adjusted duty cycle after the addition element. D is nominally .5 when the loop is locked. This represents a duty cycle of .159, (the area under the normal curve greater than 1σ), plus an offset of .341 (the area under the normal curve between 1σ and 0, represented by the adder element.) There are positive and negative inputs at the comparators. Note that because the threshold for comparison $V_{1\sigma}$ is set higher than the mean of the input signal, the high/low duty cycle of the loop comparator will be less than .5. In reality, A is a more complex transformation, representing the fraction of time $V_{in}$ is above $V_{1\sigma}$, and K is the inverse transformation, generating $V_{1\sigma}$ from D (or rather, a product of the difference between D and it's nominal value.) The feedback loop should force the value of D toward .5. From the diagram, construct the equation:

$$D=A(V_{in} - KD) + .341 \quad (1)$$

Which can be manipulated into

$$D(1 + AK) = AV_{in} + .341 \quad (2)$$

It is assumed that the gain of the product AK is greater than 1, so the 1 in this equation can be ignored. 1+AK in an actual circuit it would represent a series of voltage maps that result in the desired offset.

$$DAK = AV_{in} + .341 \quad (3)$$

We can also see from the diagram that $DK = V_{1\sigma}$, the feedback value.

$$AV_{1\sigma} = AV_{in} + .341 \quad (4)$$

There is some confusion in this interpretation surrounding the blocks A and K. The combination of the comparator marked A and the duty cycle detector maps the signal into a kind of σ-space, where it can be compared to the value of 1σ, which has been stated as .159, but not in volts. What this number represents is 15.9 percent of samples. Likewise, the value of D=.341 in σ-space is not a constant voltage, but merely a value representing the fact that the mean of the input samples will be 1 standard deviation less than KD. After the addition element, block K likewise maps the signal D from σ-space back to the same space the input voltage is in, so that they may be compared. Hence the input comparator is comparing the samples to the average value of the samples plus 1 standard deviation.

So, to explain equation (4), the transformed $V_{1\sigma}$ should be 1 standard deviation (.341) above the mean of $V_{in.}$ The A transformations simply indicated that the values are being compared in σ-space rather than voltage space. This loose linear interpretation of the algorithm is strictly for understanding, and does not reflect the actual operation of the circuit, which is not entirely linear.

In an actual circuit, a mean duty cycle of .5 could be realized by a charge pump with equal source/sink current values. Such a pump would be stable if the input duty cycle were exactly .5, and could be driven to the stable value by the feedback action of the loop.

The duty cycle measurement makes this loop more similar to a phase locked loop than a traditional feedback system. Harrison [2] interprets the duty cycle block as an integrator. Furthermore, the amplifier K translates the duty cycle value, which is nearly DC, into a usable $V_{1\sigma}$, and therefore is better described as a voltage map than an amplifier. In that case, the value of $V_{1\sigma}$ that K generates changes very slowly, and reacts only to changes in the duty cycle over a long period. This is desirable for the application described in this paper.

If the duty cycle is too low, the value of $V_{1\sigma}$ will drop to allow the duty cycle measurement to rise. If the duty cycle is too high, the value of $V_{1\sigma}$ will rise and the duty cycle measurement will drop.

Once an appropriate value for $V_{1\sigma}$ is settled on, an appropriate spike threshold can be chosen. The multiplier N represents the number of σ units away from the mean at which the spike threshold will be set. For example, if N=3 is chosen, the value 3σ is used as a threshold. Only .135% of Gaussian samples will lie above this threshold. Therefore, it is very unlikely that the noise on $V_{in}$ will trigger the spike comparator, unless some external event causes the signal to rise significantly in voltage. This event is the signal spike that the system is trying to detect.

An example of 1σ and 3σ thresholds is shown in figure 2.3, along with the probability density function of a Gaussian random variable:

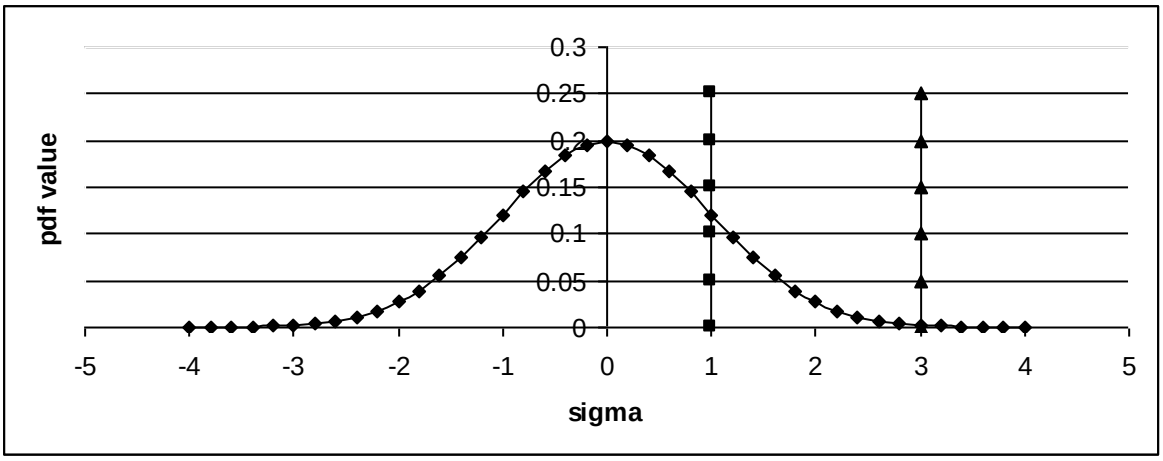



**Figure 2.3. Gaussian distribution with 1σ and 3σ levels marked.**

The 1σ value is at sigma=1. 15.87% of samples will be larger than this value.

The 3σ value is at sigma=2. Only .1350% of samples will be larger than this value.

While the general algorithm presented by Harrison is a novel and potentially useful feedback algorithm, it has not been implemented as an implantable IC ([2], [3]) and uses an external power source. A later work by Harrison [5] does in fact utilize a fully implantable IC, powered wirelessly by inductive coupling, although there is no automatic threshold detection on-chip. Instead, the chip allows a 15 kbps digital representation of a single channel (of the 100 channels) to be selected and transmitted, while an external device computes and sets an appropriate threshold. Table 2.1 compares this chip to the UTD wireless implantable chip.

**Table 2.1. Univ. of Utah INI chip [5] and Univ. of Texas at Dallas Wireless Implantable Chip**

| | INI chip - Harrison | UTD Analog Design Team |
|---|---|---|
| CMOS Process | .5 µm | .18 µm |
| Chip Dimensions | 4.7 x 5.9 mm | 2.7 x 5.7 mm |
| Neuron Channels | 100 | 128 (64 differential channels) |
| Connection to Nervous System | Central nervous system probe array | Peripheral nervous system, nerves stimulated to grow into contacts. |
| Overall Power Consumption | 13.5 mW | <500 µW |
| Data Transmission | Wireless, inductive coupling | Wireless, inductive coupling |
| Data Reduction Strategy | Select and monitor single channel, set spike threshold externally | Automatically measure noise and set spike threshold internally |

The primary advantage of the UTD chip is the power consumption, which is an order of magnitude lower. This is critical when attempting to build a system that is powered wirelessly. Also, heat dissipation is a problem in biological systems, as a temperature change of a few degrees Celsius can cause the surrounding tissue to die. The UTD chip is also slightly smaller due to the process used, and is intended to connect to peripheral nerves rather than the central nervous system.

## 2.3 Approach to Generating a Threshold Level

The nature of the input waveform is that spikes (large voltage peaks) occur generally not more than once every 10 milliseconds, lasting about 1 millisecond. Flexibility must be built in for spikes of varying duration and/or frequency. The other 90+% of the time (more if the nerve is not firing constantly), noise is present on the input line coming from the nerve. It is therefore reasonable to make assumptions about the noise level based on the calculated RMS level of the overall signal. Therefore, the first goal of the circuit is to calculate the RMS level of the incoming nerve signal in real time.

The threshold for a nerve spike can be set as a multiple of RMS voltage, such as three RMS's, or five. It is reasonable to assume that RMS level of the signal is dominated by noise, and largely ignores nerve spikes.

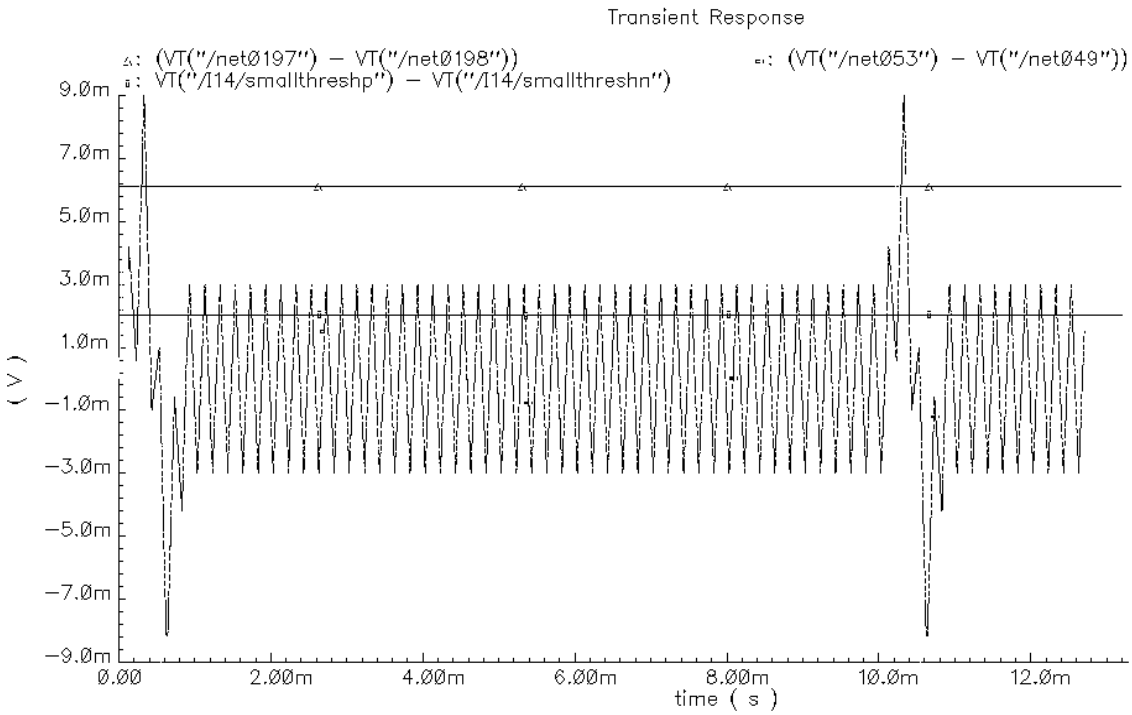



**Figure 2.4. Example of 1σ and 3σ thresholds for a noisy signal with spikes**

The spikes in figure 2.4 occur at about .7 ms and 10.7ms. The rest of the variation is assumed to be noise. If the RMS level of the signal is calculated over a large sampling period, the impact of the larger spikes on the calculated value will be minimal. So, using an integration based technique, one can calculate the approximate RMS level of the signal, which is assumed to be close to the level of the noise. The lower line shows the calculated RMS level.

Based on this RMS level, a higher "spike threshold" level can be postulated, which will be used to determine which potential differences are actually nerve spikes, and which are simply noise coming from the channel.

# CHAPTER 3

# CIRCUIT DESIGN

The circuit proposed in [2] generates a single ended threshold value. Because the power supply on the wireless implantable chip will be fairly noisy, it is necessary to create a fully differential detection system to improve power supply rejection. Therefore, since the input will be differential, the generated threshold(s) must also be differential, and the comparators and amplifiers used must be fully differential as well. Digital segments of the algorithm, notably the duty cycle measurement, need not have a fully differential implementation, since they have relatively low performance requirements.

The proposed circuit structure for the Adaptive Threshold using Noise RMS, hereafter called ATNR, is shown in figure 3.1.

## 3.1 Implementation

The ATNR was implemented in a monolithic circuit using the TSMC .18 micron process. It includes schematics and a layout for the finished product, developed using the Cadence software package, 5.0.0. All components were designed by hand; no library blocks were used. The ATNR block was laid out on the same chip as the rest of the system components, but with its own set of pin connections. In theory, if every component on the chip were to work exactly as predicted, the fabricated chips could be used for the application for which they were designed by connecting the ATNR input pins to the outputs of one of the channel amplifiers, and using that

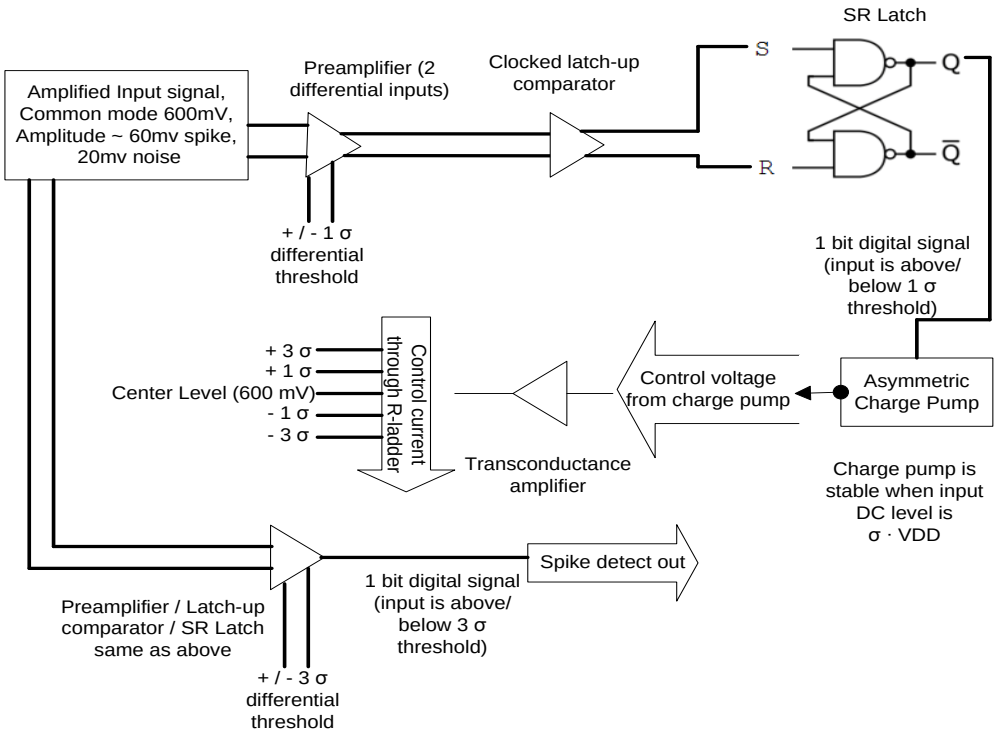



**Figure 3.1. Proposed ATNR block level**

signal to generate the thresholds. Voltage and current references for the ATNR block are available on chip from the power block, but are not connected in the version of the chip undergoing testing. For the sake of caution, the ATNR component was separated and can be accessed independently.

### 3.2 Definition of Blocks

The input is assumed to be amplified at the start. The 70 dB amplifier was designed by a peer working on the wireless implantable chip. The input is a differential signal with a common mode of 600 mV, and a spike amplitude of about 60 mV. The noise is anticipated to be about 20 mV peak to peak. Realistically, the circuit must be able to adapt the threshold to accommodate noise values from 7 mV to 60 mV, since it is difficult to anticipate how much noise will be present in a biological nervous system.

The preamplifier is a differential amplifier with 2 sets of NMOS inputs, and diode-connected PMOS loads. An NMOS (not shown) receives the 100n bias current at pin Vbias. It's dimensions are chosen to keep the device out of the deep subthreshold region, since precision is important at this stage. The NMOS5 and NMOS6 current source transistors (shown) mirror the 100n current. Because the amplifier is not connected in a feedback configuration, care must be taken to limit the gain. The purpose of this preamplifier is only to combine the input signal with the 1σ threshold without distortion, not to provide any sort of substantial gain. Once this combination has been performed, the flash comparator resolves the outputs from the preamp to determine if the 1σ threshold is greater than or less than the input voltage, acting as a simple 1-bit flash ADC. An SR latch is then necessary to remove the reset-high "teeth" from the signal

The asymmetric charge pump in figure 3.1 functions as both the duty cycle detector and the sigma adder (+.159) shown in figure 2.2. It is a duty cycle detector because, as a charge pump, it is essentially an integrator with digital inputs. It is also the sigma adder due to it's asymmetry. More current enters the charge pump on a high signal than leaves the charge pump on a low signal. If the ratio were 1 to 1, the detected duty cycle would be 50%. However, because it is not, the duty cycle is 50% plus 1σ. See the description of the charge pump for more details.

The current ladder is an analog to analog map, essentially converting the output level of the charge pump into the 1σ and 3σ differential threshold values required by the circuit. Output buffers follow to make the threshold values usable.

### 3.3 Preamplifier

The preamplifier, shown in figure 3.2, is a differential amplifier with 2 sets of NMOS inputs, and diode-connected PMOS loads. Because of the diode loads, the amplifier only has a

gain factor of about 1.2. This is desirable, because the output common mode level in a higher gain amplifier would be difficult to control without common mode feedback. The minimum feature size was selected to be 1u, to minimize variations in device parameters (particularly the channel length modulation constant) between transistors.

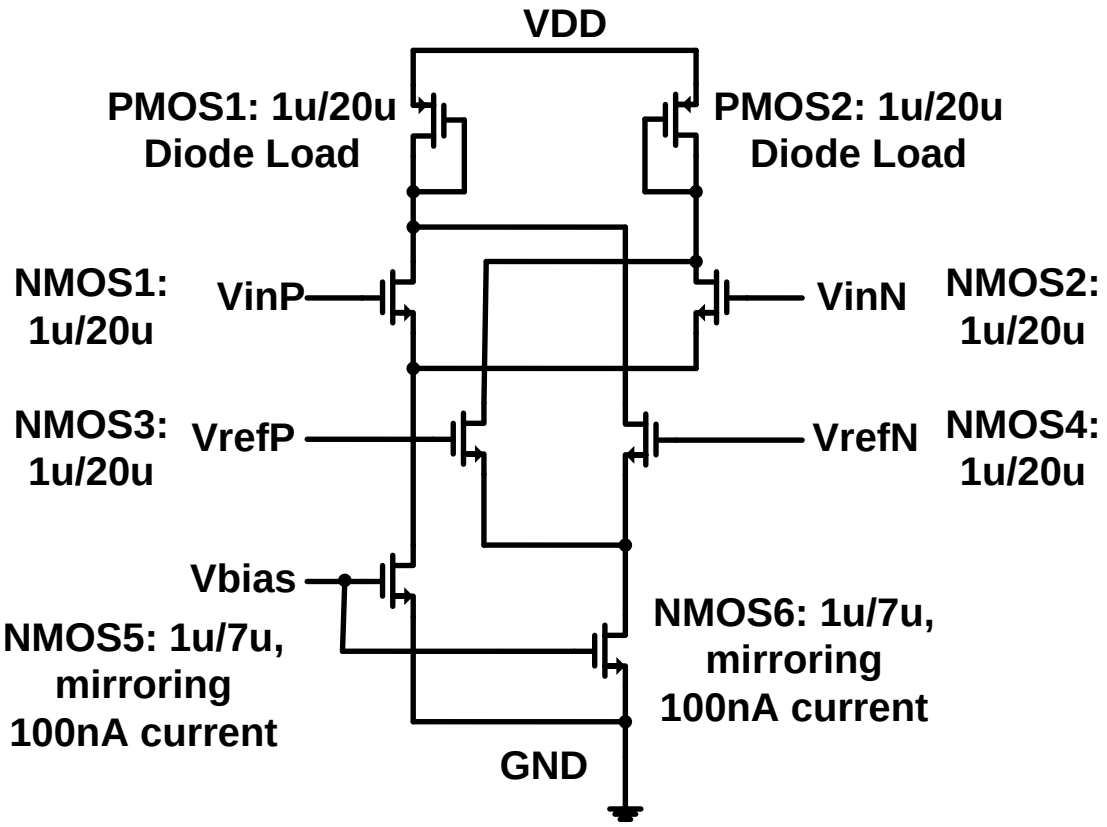



**Figure 3.2. Preamplifier**

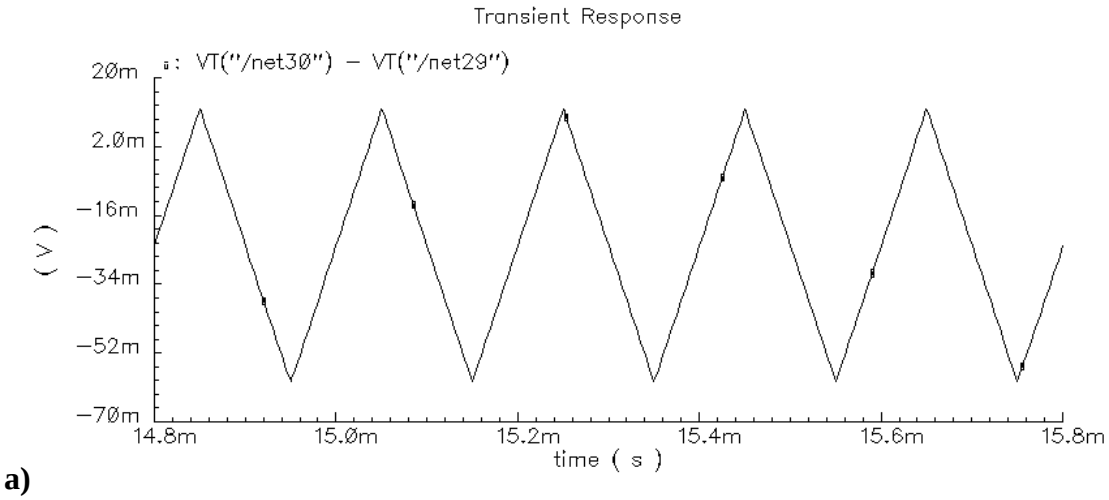
The $V_{inP}$ and $V_{inN}$ inputs correspond to the differential signal $V_{in}$. They are connected to a single current sink to improve common mode rejection. The $V_{refP}$ and $V_{refN}$ pair have their own current sink. If the sinks function as ideal current sources, common mode variations in either pair should be rejected. Simulation shows that the inputs $V_{refP}$ and $V_{inN}$ can be switched without significantly affecting the common mode rejection ratio, as long as there are 2 independent

current sinks. To illustrate the point, the transient outputs from the amplifier given a triangle wave input are shown in figure 3.3, first with no common mode variation, then with a 50 mV 10 kHz sine wave common mode variation in $V_{ref}$, and finally with the common mode variation, but only one current sink for all 4 inputs.

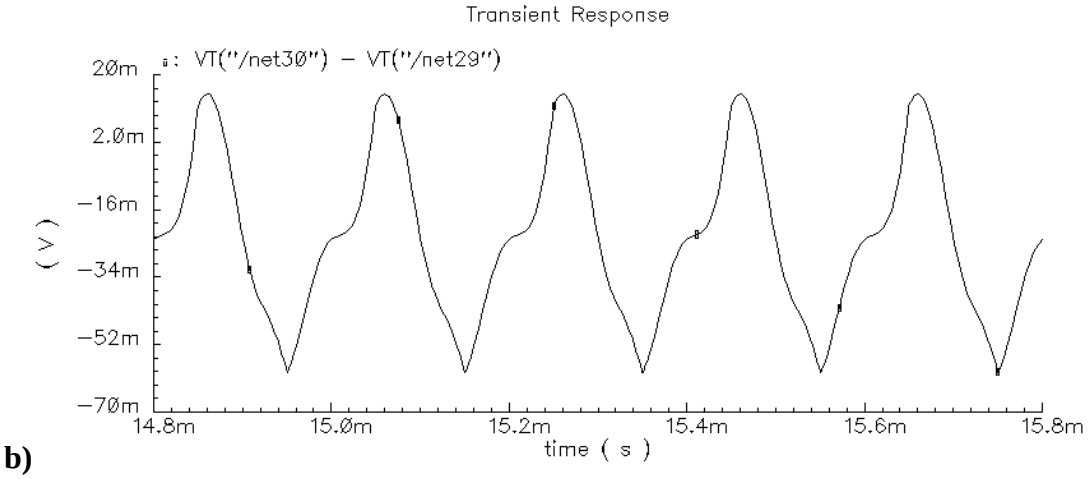
### 3.4 Clocked Latch-up Comparator

The comparator structure is a low power, high resolution design intended for use in very low power flash analog to digital converters [7]. This is critical on the wireless implantable chip, which has a very limited power supply, but especially critical for a digital subcircuit due to the limited stability of the $V_{DD}$ rail. Since no off chip capacitors are available, the power supply has a limited capacitance with which to maintain $V_{DD}$. Excessive periodic or sporadic current draw (chopping) from digital circuits must be avoided. Current steering digital circuitry, while it would alleviate the chopping problem, has been ruled out due to its high power consumption.

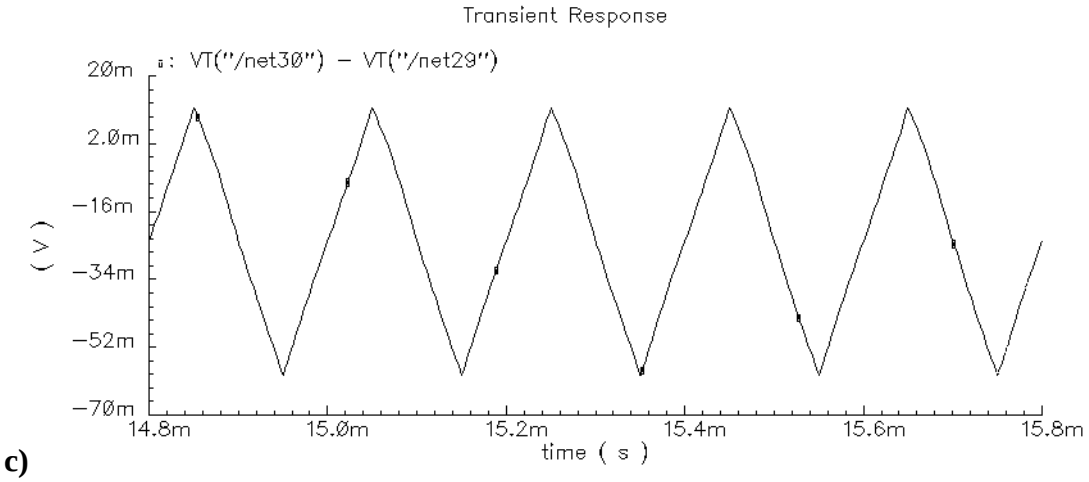
Figure 3.4 shows that this topology has 2 cross coupled pairs; one pair to pull up, and another to pull down. PMOS gates reset all 4 floating nodes by shorting them to $V_{DD}$ when the clock goes low. When the clock is high, current flows through the sink NMOS at the bottom, and through 1 of the 2 branches of the comparator, either the left side if the $V_{in+}$ signal is higher than the $V_{in-}$, or the right side if the opposite is true. The cross coupled pairs dictate that current must all flow through one branch in the steady state; it is impossible to maintain equal voltages at $V_{out+}$ and $V_{out-}$ if any amount of noise is present at the inputs. That is because latch up comparators like this one always resolve the difference between $V_{in+}$ and $V_{in-}$ all the way to the power rails $V_{DD}$ and GND.




**a)**




**b)**




**c)**

**Figure 3.3. a) Output with no input common mode variation; b) With 50 mV input common mode variation and only one current sink for all inputs, demonstrating failed common mode rejection; c) Output with 50 mV input common mode variation and separate current sinks for each pair of inputs**

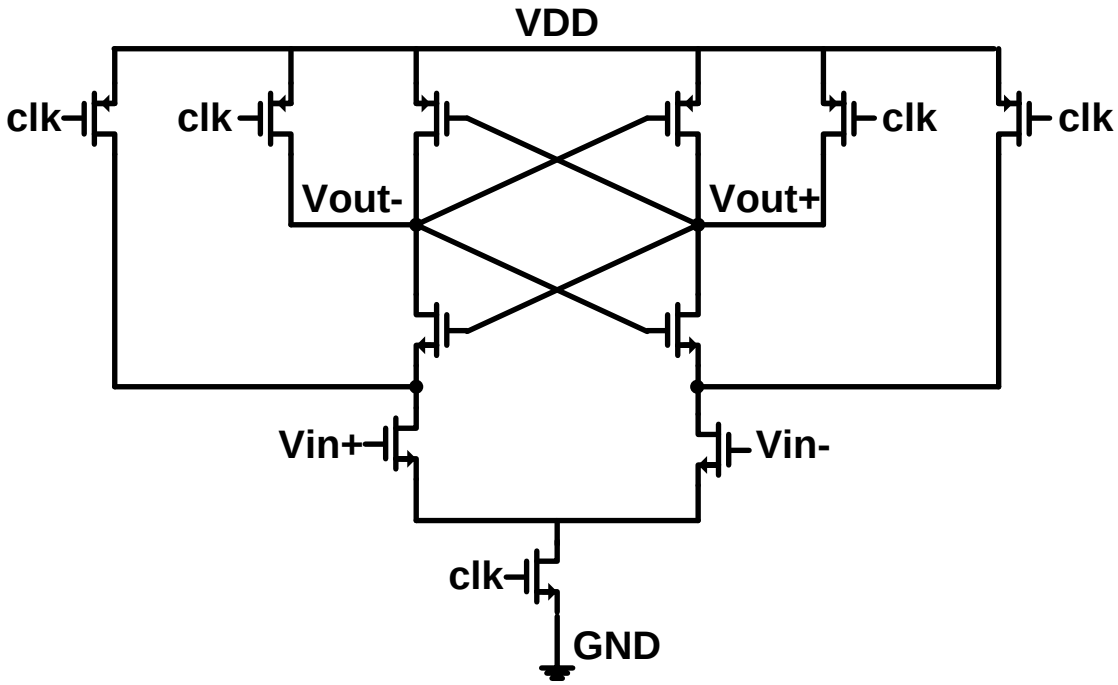



**Figure 3.4. Proposed clocked latch-up comparator**

The reason for having 2 cross coupled pairs is power consumption. When one side of pull up network (the cross coupled PMOSs) is conducting, the corresponding side of the pull down network (the cross coupled NMOSs) cannot be conducting. This way, $V_{DD}$ never has a low resistance path to ground, just as in static CMOS logic. In fact, the circuit conducts almost no current at all when it is in the latched up state. The only time the circuit uses power is when the clock goes from low to high. This is advantageous in a circuit where power is critical. The number of samples taken on $V_{in+}$ and $V_{in-}$ can be adjusted to reduce power consumption.

Because this is a digital circuit and analog precision on the output is unimportant, the minimum feature size is chosen to be 180nm, the minimum feature size of the process. Input referred accuracy is important, so PMOS resets are used on all 4 nodes that reset to $V_{DD}$, rather than just the outputs.

The cross coupled PMOSs and NMOSs are sized at 4u/180n since simulation shows that performance for these sizes is more than adequate. The NMOSs have a stronger pulling power than the PMOSs, but the pull-down action is ultimately what must cause the circuit to resolve the two inputs, and so should be the strongest. The two NMOS inputs connected to $V_{in+}$ and $V_{in-}$ are sized at 6u/180n so that they are not the bottleneck, which in this circuit is the 4u cross coupled NMOSs. The 8u/180nm clock-controlled NMOS at the base is sized to match the cross coupled NMOSs. Similar size-matched PMOSs reset the upper nodes to $V_{DD}$ on every clock cycle. The result is a clocked comparator that far exceeds the 16 kHz sampling requirement, and provides good precision.

### 3.5 SR Latch

Because the comparator latches up, it must reset between each sample. During this reset, both outputs will be high, which is an invalid state for a differential comparator, so the comparator outputs must be ignored during the part of the period when the clock signal is low.

To accomplish this, a NAND type SR latch is utilized, of the type shown in figure 3.5.

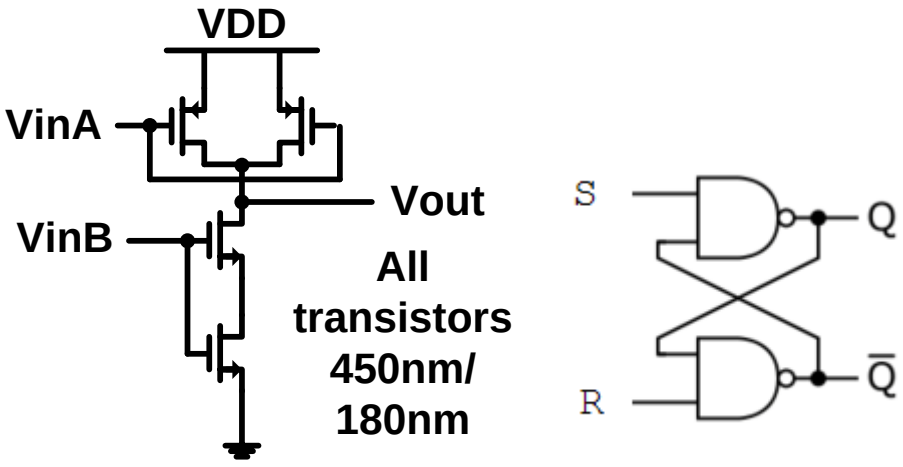



**Figure 3.5. NAND SR-latch**

The outputs from the comparator, $V_{out+}$ and $V_{out-}$, are connected to the S and R inputs on the SR latch. The SR outputs, Q and Qnot, are always opposite in value. The SR latch effectively ignores the inputs when both are high, using the memory cell to maintain the previous values for Q and Qnot. This is illustrated in a snapshot from Cadence in figure 3.6.

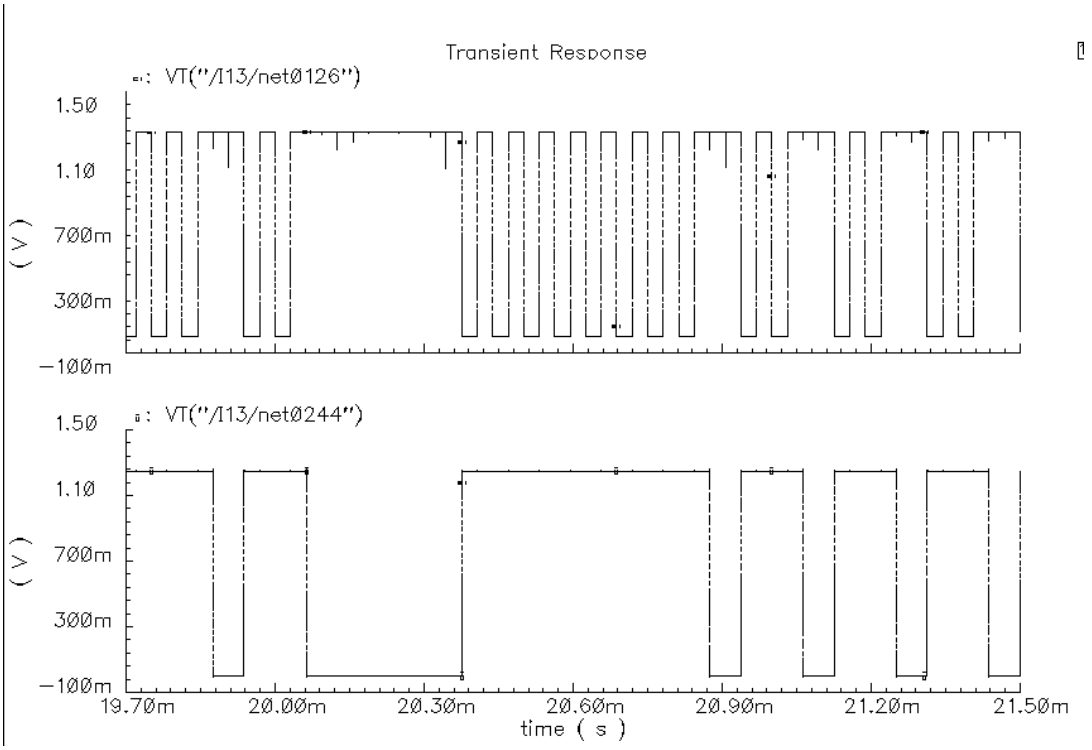



**Figure 3.6. Effect of SR latch on reset-low digital signal**

In figure 3.6, the upper waveform represents a possible output from the $V_{out+}$ output of the latch-up comparator. This output would ideally be high whenever the $V_{in+}$ input of the comparator is higher than the $V_{in-}$ input of the comparator. However, those inputs are changing very slowly, and you can see that the waveform is returning to $V_{DD}$ on every clock cycle to reset the comparator for another sample. The $V_{out-}$ waveform is similar, resetting to $V_{DD}$ at the same time every period that the $V_{out+}$ waveform does. However, during the sampling half of the period, the $V_{out-}$ waveform will have the opposite value.

The lower waveform, which is the output from the SR latch, removes these "teeth" from the signal. It simply goes high whenever the $V_{out+}$ signal goes low, and goes low whenever the $V_{out-}$ signal goes low. Therefore, the SR latch outputs a simple 1 bit representation of the output of the comparator, with no "teeth".

The NAND-type SR latch uses transistors that are sized close to the minimum allowed by the process, since NAND-2 gates are extremely fast. The NMOSs have the same dimensions as the PMOSs, based on the assumption that the NMOSs have at least twice the pulling power that the PMOSs do. Therefore, 2 NMOS gates in series will conduct roughly the same amount of current as 2 PMOS gates in parallel. Again, the performance of this digital component far exceeds the requirements of the circuit.

### 3.6 Asymmetric Charge Pump

This circuit utilizes a charge pump as an integrator, instead of a lowpass RC filter as in [2]. It improves loop performance in much the same way as a charge pump improves performance in a phase-locked loop. Furthermore, because the area of the circuit is at a premium, and no off chip capacitors are available, the charge pump allows the tracking characteristics to be adjusted by changing the current sources charging the capacitor, rather than trying to change the RC constant of a passive filter by using a larger resistor and/or capacitor. The schematic is shown in figure 3.7.

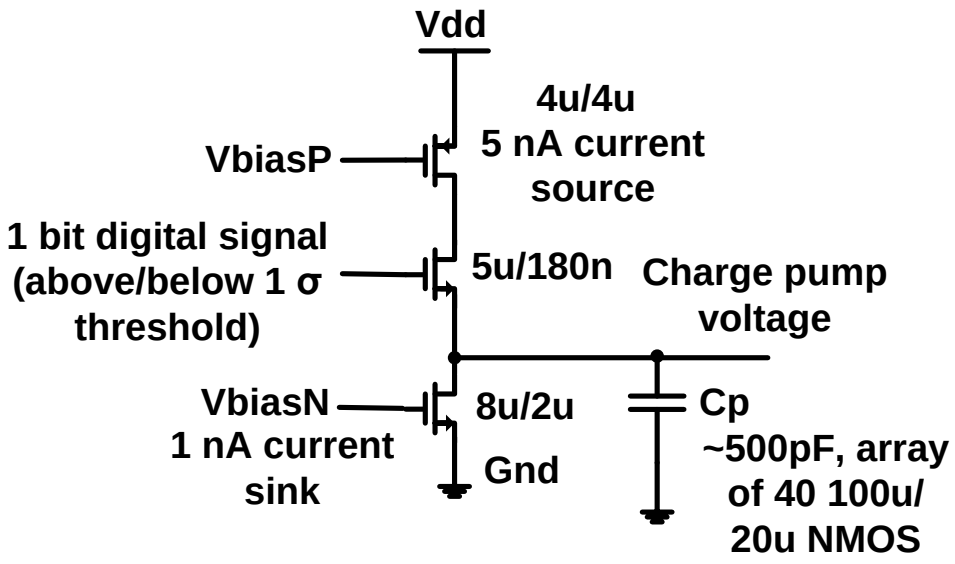



**Figure 3.7. Asymmetric charge pump structure**

The circuit is called asymmetric because the current source driving current into the capacitor $C_P$ drives more than the current sink pulling charge off of $C_P$. This is effectively where the constant .159 is added to the equation. In this case, the constant is actually .25, but this doesn't matter, since the value obtained still allows calculation of the rms value of the noisy input signal. This does mean that for purposes of this circuit, 1σ is defined as the level above which 25% of signal samples fall, rather than 15.9%. Using a 1 to 6 current ratio instead of 1 to 5 will result in a value closer to the expected σ, which would be 1 standard deviation from the mean (common mode) level. However, an exact calculation of the standard deviation is unnecessary, because in theory any value other than 100%, 0%, and 50% will allow the calculation of an appropriate spike threshold. This is because 100% and 0% levels could be arbitrarily high or low, and the 50% level would only allow calculation of the approximate common mode of the signal, which is already known.

The faster current inflow allows the capacitor to charge up quickly from 0 Volts, improving operating performance. This can be considered a fast attack/ slow recovery operation.

It is assumed that if the proposed 1σ threshold value is very close to the measured 1σ threshold value, the voltage on $C_P$ will not change. This will be referred to as the "locked on" state. The voltage on the $C_P$ will remain steady if the average amout of current being pumped into it is equivalent to the average amount of current being pulled out of it. In this configuration, that means that the current gate MOSFET G must be open one fifth of the time. Hence the constant .20, rather than .159. This gate is controlled by one of the signals from the SR latch, which is a bit indicating whether the proposed threshold is too low or too high. Therefore, it is assumed that in the locked on state, this bit will be low (gate open) one fifth of the time.

When gate G is open, the net current flow into the capacitor is 5nA -1nA = 4nA, or -4 times the value when gate G is closed. If the gate is open only one fifth of the time, there will be a steady charge on $C_P$ across 5 hypothetical clock cycles:

(gate open current flow) – 4(gate closed current flow) = 0nA

(5nA – 1nA) - 4(1nA) = 0nA

So if there is no net current flowing into or out of capacitor $C_P$, the charge will remain the same on average.

The other asymmetry in the circuit is that there is no gate on the 1nA current sink. Such a gate could easily be driven by the other output from the SR latch. However, it would do little for the performance of the charge pump, because ripples in the voltage on $C_P$ are caused by the switching of the net current amounts into/ out of $C_P$, which would still occur if 2 gates were present. Some small current might be saved, but the charge pump is already using much less current than the rest of the circuit by a large margin; 5nA vs nearly 2uA total.

In summary, if gate G is open 20% of the time, net current flow into $C_P$ will be 0, and the voltage on $C_P$ will remain constant. If gate G is open less than 20% of the time, net current flow

into $C_P$ will be less than zero, and voltage will drop. Likewise, if gate G is open more than 20% of the time, the capacitor will charge (quickly). Because the voltage on $C_P$ indirectly sets the proposed 1σ threshold, lower or higher voltages on $C_P$ will result in the input signal at gate G being low (gate open) more or less often, thus creating the feedback that enables this circuit to lock on to an appropriate threshold voltage.

The upper PMOS component PM2 is sized to be an ideal 5nA current source, and is tied to a diode connected 4u/4u PMOS elsewhere in the schematic in a current mirror configuration. This ensures good 5nA reproduction. The NMOS NM2 is configured similarly to act as a 1nA current sink. However, only the 5nA source is modulated by a t-gate, implemented by the second PMOS connected to the "ctrl" line. This gate ensures that the 5nA current only flows into the capacitor when the ctrl signal is low. It has a short, wide channel to ensure a low "on" resistance.

The main component of the pump is the 500 pF capacitor, implemented by a parallel array of 40 17pF capacitors, the largest permitted by the process. These capacitors measure 100u x 23u apiece in layout, for a total area of 1020u x 90u. This capacitor is larger than many integrated circuits. The reason for this large capacitor is that there is an engineering tradeoff between the input current and the size of the capacitor. The voltage ripple on the top plate of the capacitor depends directly on the ratio I/C, where I is the amount of current flowing into or out of the capacitor at any given time, and C is the capacitance. The current I has already been reduced to a very small amount, 5nA from the source and 1nA into the sink. Tools that can determine the lowest current level that can reasonably be assured in this process are unavailable, so it would be unwise to use any current lower than 1nA. In other words, choosing 50fA could result in incorrect operation if process variations caused the actual current value to be 550fA, or

even 0fA. Therefore, the only way to keep the voltage ripple low (and thereby keep the threshold levels steady) is to choose a very large capacitor.

The capacitor functions as a 500pF capacitor only above 470mV. Below this, approximately 30% of the capacitance is lost. While this does help the circuit charge up more quickly from a zero-voltage state, it has the unfortunate effect of reducing the stability of the capacitor voltage, and therefore the stability of the threshold which is output. It is for this reason that a minimum threshold is defined. If an input signal causes the capacitor voltage to drop too far into this region, the 3σ voltage will not fall below 6mV. If testing proves this value to be too low, it can be modified in a later revision of the circuit.

### 3.7 Current Ladder

The current ladder portion of the circuit consists of three parts: a source- degenerated NMOS transconductance amplifier, a resistor ladder which acts as a load for that amplifier, and a voltage regulator that keeps the center node of the ladder at the common mode level for the circuit, in this case 600 mV. These can be seen in figure 3.8.

The source degenerated common source amplifier allows the gain to be controlled with much better accuracy than a non source degenerated amplifier. AC gain (transconductance) is approximately 1/R5. DC biasing can be accomplished by calculating the source to drain current flow through the NMOS. This simple amplifier functions as an ideal current source for purposes of this circuit.

It is assumed that R2 = R3, and that R4 = R1. Furthermore, R1 = (N-1)*R2, so the value of N is determined by the choice of resistors in the ladder. (The ATNR circuit feeds the 1σ level back to itself, while outputting the N-σ level.) The resistors must all be fairly large to allow for a small current in the ladder. This creates a tradeoff between power consumption and area. At 50

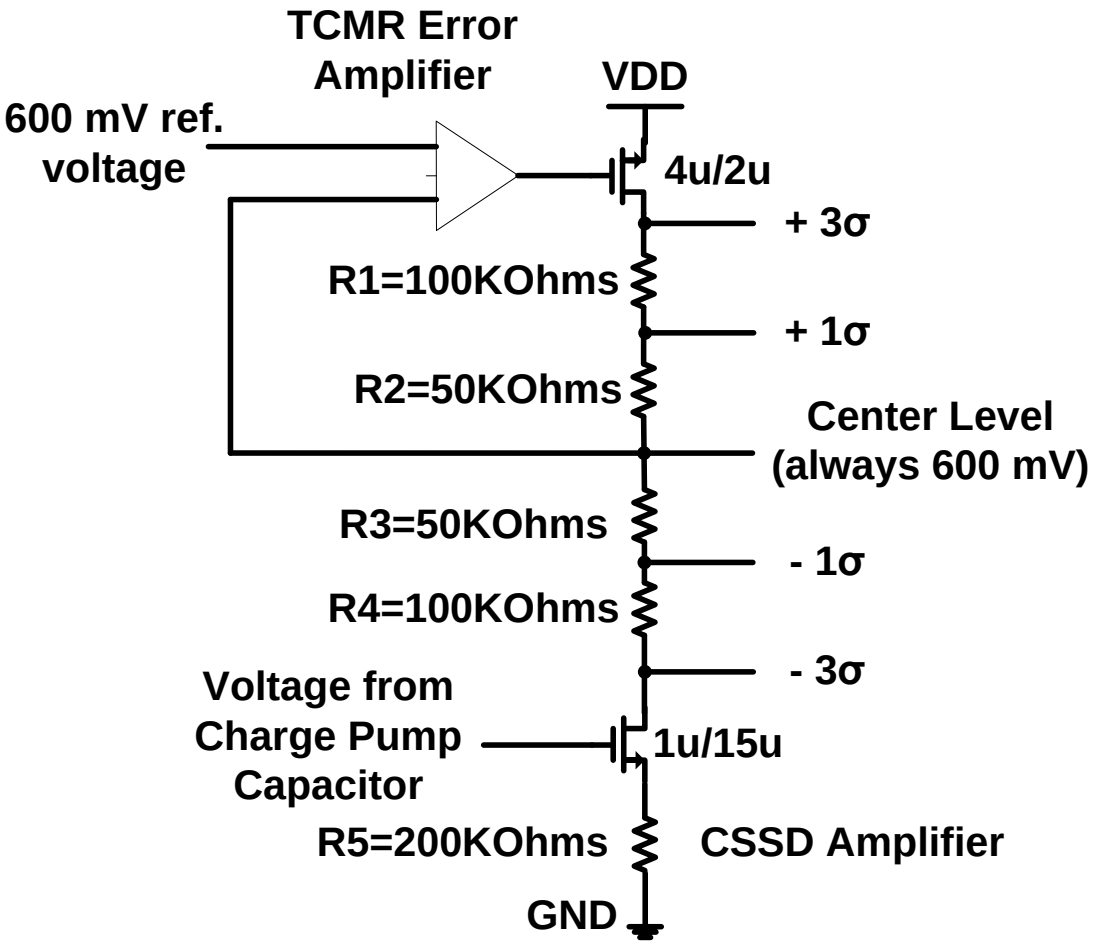



**Figure 3.8. Current ladder**

kΩ to 100 kΩ, polysilicon resistors start to become very large. It is this circuit element that consumes the majority of power in the circuit's budget. This is a place where the design can be improved significantly in future iterations.

So with a defined amount of current Ia flowing through the ladder, and the center level between R2 and R3 assumed to be held constant at $V_c$, the voltage levels at +1σ and -1σ are equal to $V_c$ (+/-) Ia*R2. If N=3, then resistors R1 and R4 would be equivalent to 2R2, and the voltages at +Nσ and –Nσ would likewise be equal to $V_c$ (+/-) 3*Ia*R2.

Note that these are the proposed values for the 1σ and Nσ thresholds; they do not necessarily reflect measured RMS values until the closed loop circuit has locked on. The 1σ

levels are fed back to the first comparator, closing the loop and checking them for accuracy. The Nσ levels are buffered appropriately, and distributed to the rest of the circuit, where they are compared to the input signals to determine the presence of a potential spike on the other inputs.

An error amplifier controls the gate voltage on the PMOS at the top of the ladder. Since this PMOS also functions similarly to a current source, when the gate is at the proper voltage to conduct the same amount of current as the NMOS amplifier on the other end, the center level $V_c$ will be near the average of the rails $V_{DD}$ and GND. The error amplifier compares $V_c$ to a reference Vc, in our case 600 mV, and adjusts the PMOS gate voltage accordingly. This structure is very similar to a low dropout voltage regulator. However, because the load of the voltage regulator is actually another transconductance amplifier, this comparison breaks down. Stability must be closely monitored, since placing a feedback loop inside a feedback loop can result in strange effects. However, in this case the outer loop (the overall detection scheme) is much slower than the internal loop (the center voltage regulator for the ladder), so this problem can be regulated. Also, because the center level is to be held constant, capacitors can be placed in several areas to stabilize any strange effects.

The NMOS and a 200K polysilicon resistor make up the common-source source-degenerated current amplifier. The transconductance is roughly equal to the inverse of the source degeneration, hence:

$$\frac{1}{200K} = \frac{5nA}{mV} = g_m$$

A second NMOS in parallel with the first conducts a constant 20nA, setting the minimum current, and therefore minimum threshold values.

The transconductance was slightly smaller when simulated. The transistor gate is connected to the capacitor in the charge pump. The transistor was then sized such that the drain

current would be approximately 200nA when the gate voltage was at the minimum level for linear capacitance on the charge pump, 470mV, using the drain current equation. Therefore, when a 600mV voltage is applied at the input, the drain current is

$$(600mV - 470mV) \cdot \frac{5nA}{mV} + 200na = 850nA$$

.

The NMOS NM5 conducts 50nA through the current ladder at all times, establishing a minimum ladder current at 50nA.

Assuming the center node, the node between the two 50K resistors, is held at 600mV, a current of 900nA results in threshold voltages of 642.5mV and 557.5mV, or 85mV differential, for the 1σ level, and 727.5mV/472.5mV/200mV differential for the 3σ threshold.

Due to the voltage regulator maintaining the center at 600mV, there is a situation where each amplifier acts as part of the load of the opposite amplifier. As a result, the gain of the CSSD amplifier is nonlinear, and tapers off at higher input levels as the load is reduced by the feedback loop of the other amplifier. This is addressed in more detail below.

It was mentioned above that as the charge pump capacitor moves into the region below 470mV, a region with smaller capacitance, voltage ripple becomes larger. However, that voltage is connected to the CSSD amplifier NM0. While conducting relatively small currents, this transistor will move deeper into the subthreshold region of operation, which at a certain point will cause $g_m$ to decrease. With the gain of the amplifier going down, the problem of increased voltage ripple is mitigated.

The PMOS PM0 supplies the current to the top of the ladder, and is gate connected to the op-amp labeled "Threshold Common Mode Regulator," or TCMR. This is a simple op-amp measuring the difference between the center node (the node between the two 50K resistors) and the ideal 600mV center level. This measurement controls PM0, which controls the amount of

current that is allowed to flow into the ladder. PM0 is sized to conduct the appropriate amount of current using the drain current equation. The gate of PM0 is connected to a capacitor to stabilize the loop.

So, the current ladder has both a PMOS current source and an NMOS current sink driving current through the branch. This is similar to the case where a simple transconductance amplifier has a biased transistor load, and therefore two current sources are trying to establish a current in the branch, except that in this case both transistors are connected to varying bias levels.

Another way to understand the circuit is to say that the op-amp TCMR is feedback connected to the center node, and constantly driving it to 600mV, but that the CSSD amplifier represents a changing load to the first (TCMR) amplifier, which the first must be able to adapt to.

Capacitors are placed on the nodes where the 1σ levels are generated to stabilize them. The values were determined by simulation, by measuring the amount of current kickback at those nodes when the circuit is fully connected, and using enough capacitance to mitigate that effect.

### 3.8 Output Buffers

The output buffers on the 3σ outputs consist of op-amps in unity gain feedback configuration. The slew rate and output capacitance are calculated to keep the voltages stable, based on the array of 64 comparators that will be connected to these outputs when the circuit is fully connected. The capacitance amounts were determined as before, by measuring the total kickback to each node, and sizing the capacitors to minimize the effect.

### 3.9 Summary of Circuit Operation

In summary, the input signal $V_{in+/-}$ is combined with the proposed +/-1σ threshold level in the differential preamplifier, and then passed on to the clocked latch-up comparator, where it is sampled at 16 kHz to determine whether the input signal is above or below the 1σ level. The result is a 1 bit digital signal $S_D$. The reset-high portions of this signal are removed by an SR latch, resulting in $S_D$`. This signal controls an asynchronous charge pump, which charges a capacitor much more quickly than it drains the capacitor, causing the charge pump to be in a steady state only when $S_D$` is low for about 20% of the time, instead of the 50% that would hold a symmetric charge pump steady. This gives an indication of how close the proposed 1σ level is to the level above which 20% of $V_{in}$ samples lie; i.e. our desired 1σ, the level to which the proposed 1σ level should be locked. The charge pump then drives the current ladder section of the circuit, which is actually a voltage map, translating the charge pump capacitor's voltage to proposed 1σ and Nσ levels. The 1σ level is then fed back to the first comparator, where it is compared again to the input signal. This feedback process continues until the proposed 1σ value has "locked on" to the 1σ value of the input signal.

The Nσ threshold is buffered and distributed to other areas of the chip, where it is compared to other inputs to determine the presence of neural spikes.

### 3.10 Chip Micrographs

**Figure 3.9. View of entire chip die.**

The large repeated structures are the input amplifiers. The ATNR is near the bottom.

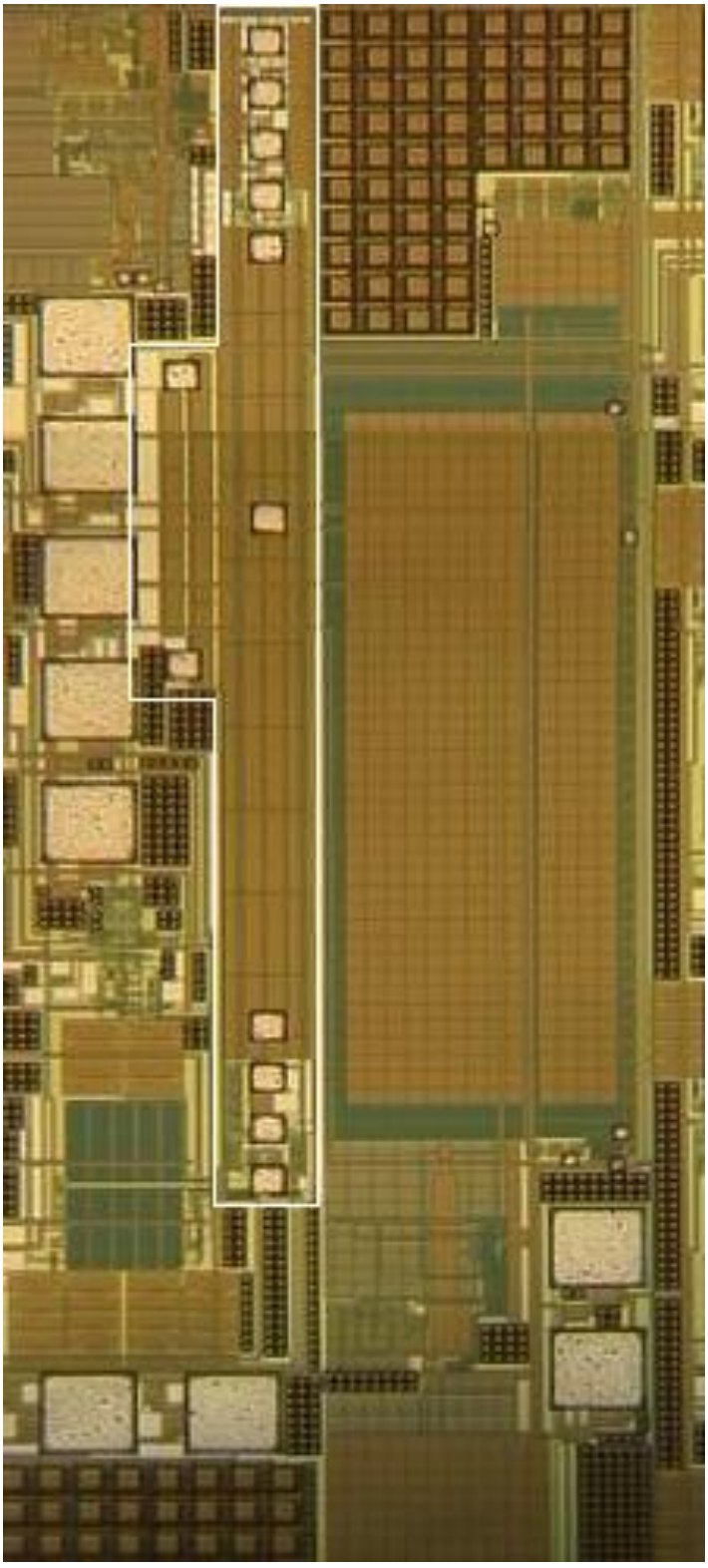


**Figure 3.10. Close-up of chip with ATNR bordered in white. Capacitors dominate the layout.**

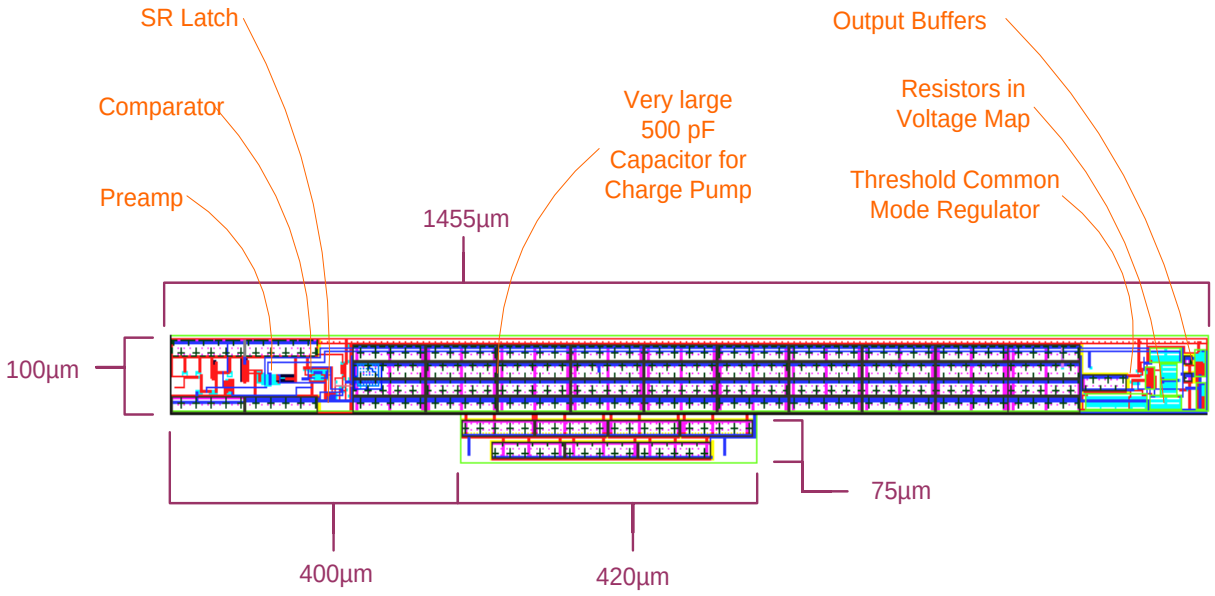



**Figure 3.11. Labeled Layout View**

Chip Area = 1455µm x 100µm + 75µm x 420µm = 1.77mm$^2$

# CHAPTER 4

## SIMULATION RESULTS

The simulations were conducted in spectre using the TSMC .18 micron library. Triangle wave generators were used to simulate noise and spikes, while at the same time making it obvious when the loop reaches a locked condition.

The simulation in figure 4.1 shows the differential 3σ threshold locking on to a 133mV peak to peak noise input, simulated by a triangle wave. Spikes are simulated every 10ms. The first strip shows the differential 3σ threshold, the second strip shows the differential input signal, and the third shows the voltage on the charge pump capacitor as the loop locks onto the signal. The 3σ threshold signal shows a ripple of 2.65mV differentially when a spike occurs in the locked condition.

It is assumed that the input has been amplified by other circuitry. The input should have a common mode of 600 mV, a spike amplitude of about 60 mV, and noise of approximately 20 mV peak to peak.

The capacitor (c) needs to charge up to about 250mV before the output (a) starts to move away from its minimum value. The input signal is a triangle wave, so as the output moves higher, the comparators trigger positive less and less often, so we see a gradual curve on (a) as the outputs level off, and finally a horizontal line at about 200ms as the loop locks to the input level.

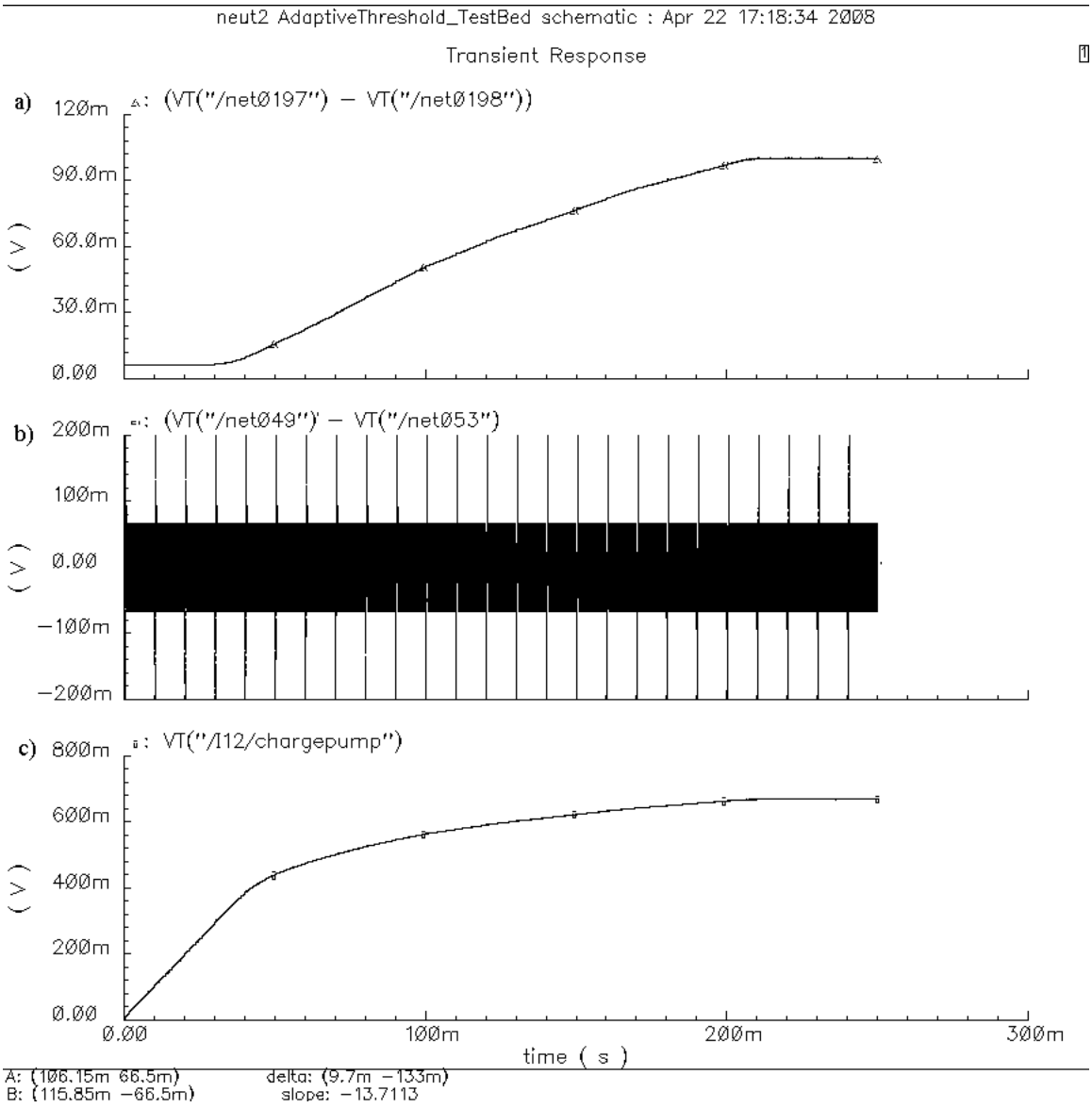



**Figure 4.1. Simulation capture: the a) 3σ threshold, b) input signal, and c) capacitor voltage as the loop obtains a lock on the RMS level.**

In figure 4.2, an artificial input signal is used to stimulate the circuit. It represents the bare minimum value at which the thresholds can be set. In this simulation, the charge pump cannot discharge any further, which results in the minimum possible outputs.

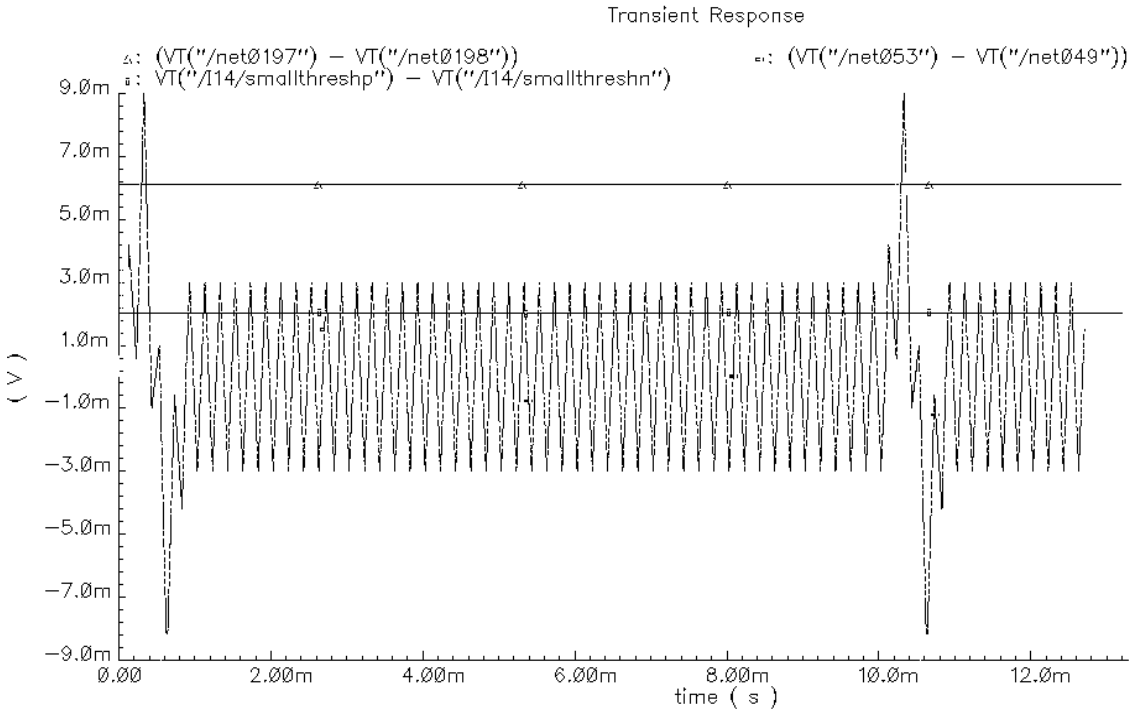



**Figure 4.2. Simulation capture: minimum possible 1σ and 3σ settings**

The "noisy" waveform is the artificial input, a triangle waveform to represent the amplified nerve signal, with spikes out to three times the amplitude of the "noise". In a biological system, spikes will be as large as 5 times the peak noise level. The line near the center is the 1σ level, which is unable to set itself any lower than 2mV differential. The 3σ threshold is therefore set to 6mV. For this setting, any samples above 6mV will be considered spikes.

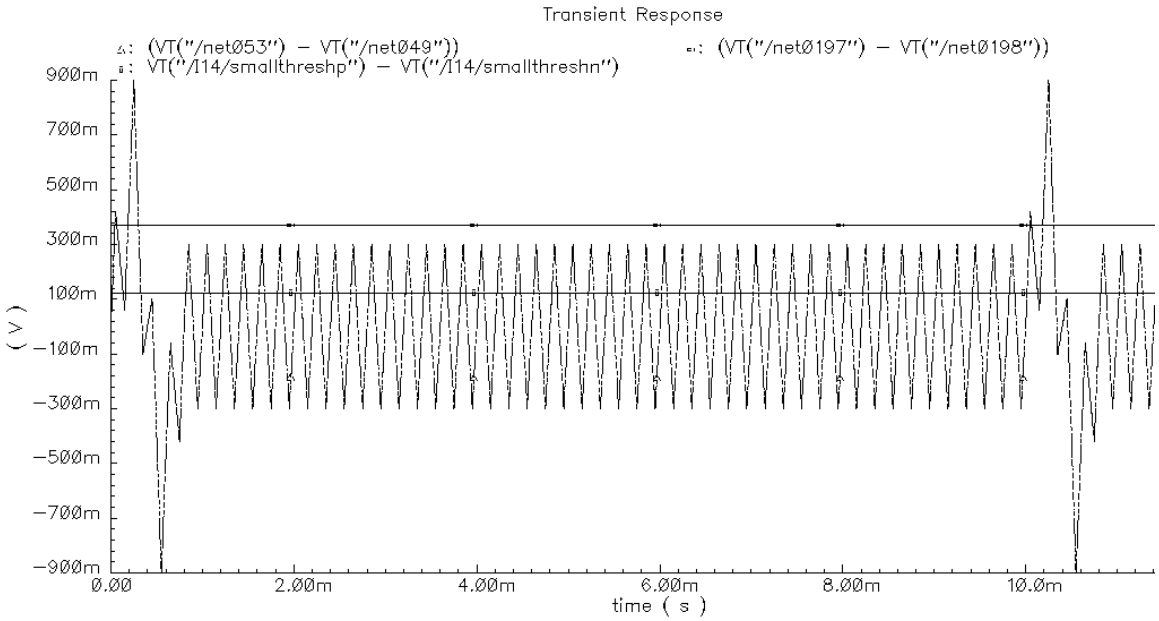



**Figure 4.3. Simulation capture: maximum possible 1σ and 3σ settings**

In this figure, the 1σ threshold value has reached its maximum at 115mV. Spikes will be compared to the 3σ threshold at 350mV.

What this demonstrates is that the 1σ threshold can be set as low as 2mV, or as high as 110mV, and the circuit will still function properly. These levels correspond to noise peaking at about 3mV and 300mV, respectively. Outside this window, the 3σ threshold will be stuck at either it's minimum of 6mV or it's maximum of 350mV.

However, simulation reveals that the charge pump capacitor is only in its linear range above 470mV, which corresponds to a 1σ voltage of 7.5mV, and a 3σ voltage of 22.5mV. Likewise, the PMOS current source charging the capacitor only operates as an ideal 5n current source when the capacitor stays below a certain level. However, it is the max locking time that will determine the largest possible input signal, as larger input levels result in longer charge times for the capacitor, and overall longer locking periods.

Therefore, for linear operation of the circuit with a small safety margin, and a max locking time of 250 ms, the peak voltage of the input noise must be between 12mV and 75mV. The output ripple will become slightly worse as the 1σ level drops below 7.5mV.

Proper operation of the circuit is demonstrated in figure 4.4.

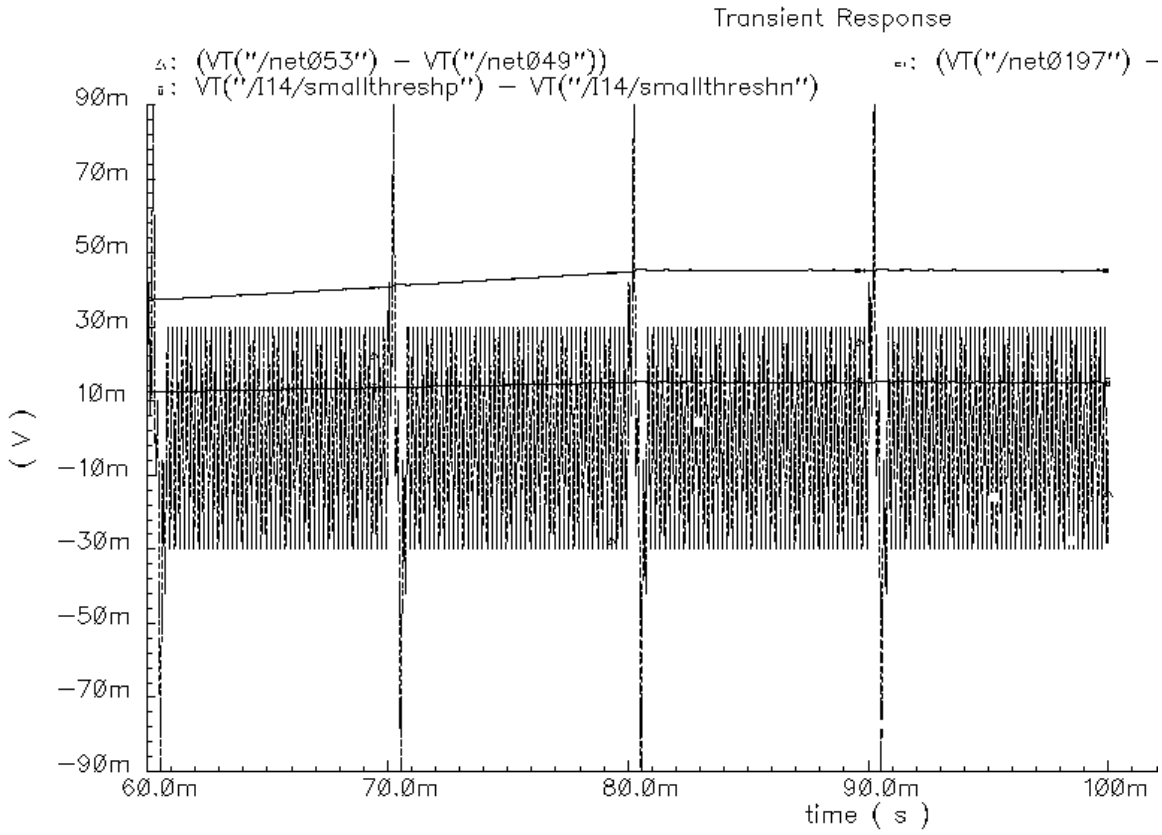



**Figure 4.4. ATNR locking to a 1σ of 15mV, and a 3σ voltage of 45mV.**

The simulation in figure 4.4 was started with the charge pump capacitor preset to 400mV. 50 milliseconds are required to charge the circuit this level. We also see that 80 ms into the simulation, the circuit achieves a lock. Thus, the total time required to achieve a 1σ of 15mV is about 130 ms. Signals with more noise will require more time to lock.

The data in table 4.1 was collected over several simulation runs. Its purpose is to give an idea of how the circuit will perform when fabricated.

**Table 4.1. Tabulated simulation results**

| Values are in millivolts unless otherwise specified | | | |
|---|---|---|---|
| Peak Noise Voltage | Spike Voltage | Locked 3σ Threshold level | Time to Lock (ms) |
| | | | |
| 3 | 9 | 6 | 0 |
| 15 | 45 | 22.5 | 85 |
| 30 | 90 | 45 | 130 |
| 45 | 135 | 67.5 | 162 |
| 60 | 180 | 90 | 200 |
| 67 | 200 | 100 | 210 |
| 75 | 225 | 113 | 226 |
| 300 | 900 | 350 | Very long |

Based on this data, it seems safe to specify a max locking time of 250ms with peak noise less than 75mV. The ATNR will lock to higher noise levels, but the locking time becomes very long, and is difficult to simulate in one pass. Furthermore, the circuit will enter a nonlinear region of operation as the current source and sink on the charge pump cease to operate as ideal sources. This will occur for a peak noise voltage below 12mV, or above 130mV. Standard linear operation will occur between these two input levels. However, operation is possible outside this region.

# CHAPTER 5

# CHIP TEST RESULTS

Because all components of the wireless implantable nerve sensor project were fabricated on a single chip, input and output pins were at a premium. The ATNR section was only allocated 8 pins, not including the global ground pin. As a result, only the basic input and output functionality of the ATNR could be tested. Intermediate signals were inaccessible.

Unfortunately, in the test sample, the output buffers produced a common mode that was slightly lower than expected, at approximately 530mV instead of the predicted 600mV. The fabricated chips did display the behavior that was anticipated, demonstrating the concept, but leaving room for improvement. The test circuit was connected as shown in figure 5.1.

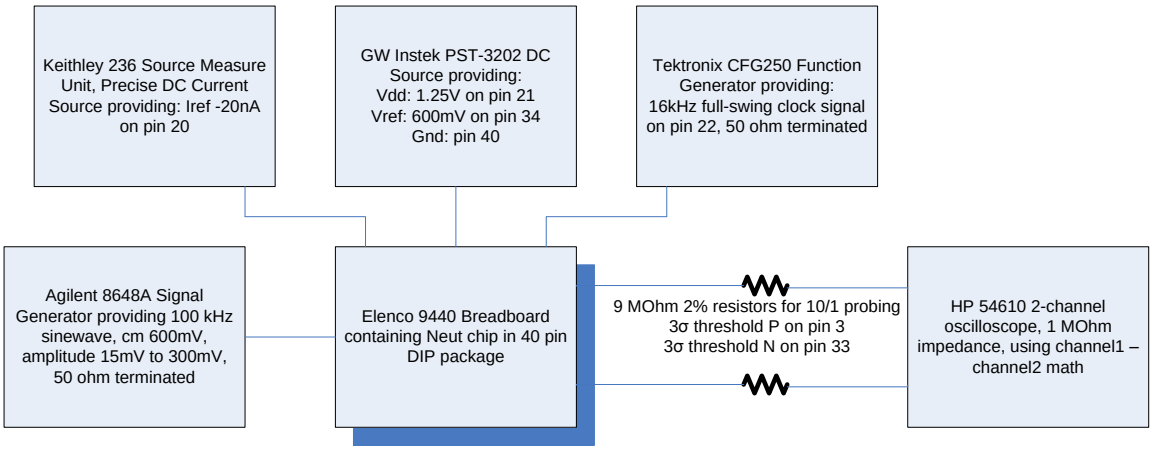



**Figure 5.1. Test Setup**

Measurements shown are adjusted to compensate for the 10/1 probe. The tests were conducted by stimulating the P-input of test sample 1 with a “noisy” signal (actually a sine wave)

and holding the N-input constant. Similar results were achieved by stimulating the N-input and holding the P-input constant.

**Table 5.1. Tabulated Simulation and Measured Results**

| Peak Differential Input Voltage | Simulated 3σ Threshold | Test Chip |
|---|---|---|
| | | |
| 3 | 6 | |
| 15 | 22.5 | 0 |
| 30 | 45 | 44 |
| 45 | 67.5 | 69 |
| 60 | 90 | 100 |
| 67 | 100 | 125 |
| 75 | 113 | 131 |
| 300 | 350 | 131 |

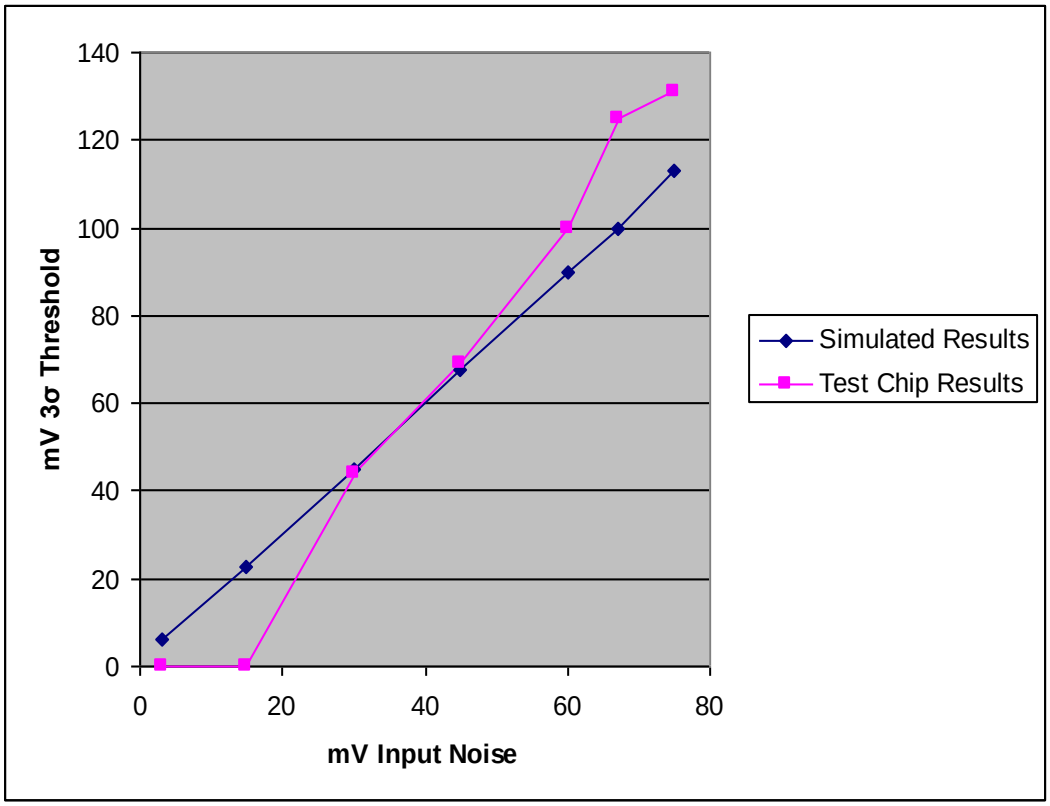



**Figure 5.2. Simulated 3σ results, and measured results from test chip**

The test chip gave results that were satisfactory, and are sufficient for proof-of-concept. Some clock noise was present on the positive and negative outputs, although it could not be

observed in the differential signal. This is likely due to some signal coupling on-chip. The slight common mode issue indicates that the output buffers need to accommodate a larger load than they presently can handle. Furthermore, replacing the analog capacitor with a digital counter should help by alleviating noise at intermediate stages. Noise at intermediate stages could not be observed due to lack of output pins, but it is assumed that some is present, since the measured results differ slightly from the simulation results. However, this could just be the result of process variation.

# CHAPTER 6

# CONCLUSION AND FUTURE WORK

## 6.1 Conclusion

In this thesis, an automatic threshold sensor for nerve sensing applications has been presented (ATNR), which utilizes the RMS level of the noise present on a given sensor to generate an appropriate threshold for detecting nerve spikes. This implementation is smaller in area and, more importantly, lower in power consumption than previous implementations. This makes the chip better suited for biological implant applications, since waste heat results in cellular damage, and lower power requirements allow the use of a power-over-wireless scheme, and ease the requirements for such a system. The elimination of wires through the skin is critical in preventing infection. Furthermore, the chip eliminates the need for an external device to set the spike threshold, as in previous implementations. It should provide an important stepping stone for those seeking to build a self contained implantable nerve sensing and transmitting device, and the low power adaptive neural spike threshold unit serves an important function in making the system self contained.

## 6.2 Future Work Overview

In order to improve the chip, its shortcomings must be addressed. The first and most glaring is the use of a very large capacitor (500 pF) fed by a very small current (as low as 1 nA at times). Current-into-capacitor solutions are subject to a significant amount of process variation. In the case of symmetric charge pumps, if both the source and sink are 1nA stronger or both 1nA

weaker, the pump still functions properly. However, because the pump is asymmetric, the ratio of source/sink currents becomes problematic. In a 5nA/1nA charge pump, the ratio could become 6nA/2nA, or worse, 4nA/0nA and cease to work at all. Because of this, it seems wise to replace the asymmetric charge pump with a digicap, or another simple digital memory device to simply track the number of high and low signals fed to the present charge pump. Once this is done, the R-ladder structure (presently an analog to analog map) can be replaced with any kind of DAC. If an R-ladder type DAC is used, it would be possible to reuse this structure and set a separate threshold for each of the 64 channels on the chip, since the voltage levels on the R-ladder could be simultaneously accessed by many different components. The digicap and other components would have to be replicated on each of the 64 channels, but the digital circuitry could be made sufficiently small that this would not be a problem. Furthermore, the use of digital circuitry would allow a set-and-forget approach that could potentially save power.

Another major shortcoming is the use of sensitive analog techniques in a chip that is essentially an RFID system. The power supply cannot be expected to be extremely stable, especially with the digital components in the rest of the chip subjecting the supply to chopping. By reducing the number of power-sensitive analog components in the loop, the ATNR's accuracy could be greatly improved.

## REFERENCES


[1] Nilsson, James W. and Susan A. Riedel, *Electric Circuits, Sixth Edition*, Prentice-Hall Inc. 2001

[2] R. R. Harrison, "A low-power integrated circuit for adaptive detection of action potentials in noisy signals," in *Proc. 2003 Int. Conf. IEEE Engineering in Medicine and Biology Soc. (EMBC 2003)*, Cancún, Mexico, pp. 3325–3328.

[3] P. T. Watkins, G. Santhanam, K. V. Shenoy, and R. R. Harrison, "Validation of adaptive threshold spike detector for neural recording," in *Proc. 2004 Int. Conf. IEEE Engineering in Medicine and Biology Soc. (EMBC 2004)*, San Francisco, CA, pp. 4079–4082.

[4] Ludwig, Reinhold and Pavel Bretchko, *RF Circuit Design: Theory and Applications*, Prentice-Hall, Inc. 2000.

[5] R. R. Harrison, et al. "A Low-Power Integrated Circuit for a Wireless 100 Electrode Neural Recording System," *IEEE Journal of Solid State Circuits*, Vol. 42, No. 1 January 2007.

[6] Stark, Henry and John W. Woods, *Probability and Random Processes, with Applications to Signal Processing*, Prentice-Hall Inc. 2002.

[7] Geert Van der Plas, Stefaan Decoutere, Stephane Donnay, "A 0.16pJ/Conversion-Step 2.5 mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process," in *Proc. 2006 Int. Solid State Circuits Conference, Session 31.1*, San Francisco, CA, pp. 566-567 and 673.

## VITA

Andrew Bruce Duffield was born in Springfield, Illinois, on January 13th, 1983, the son of Bruce Edward Duffield and Marjorie Louise Duffield. After receiving his diploma from Clear Creek High School, League City, Texas in 2001, he accepted an offer to study at the University of Texas at Dallas. He received the degree of Bachelor of Science in Electrical Engineering with an emphasis in Microelectronics. Following his graduation, he remained at the University to complete his Master of Science degree, also in Electrical Engineering, with the same emphasis. He also became a member of the Analog Integrated Circuit Design Group, studying under Dr. Jin Liu, and completed his thesis work as a part of that group.